# VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD B.E. (IT: CBCS) III-Semester Supplementary Examinations, May/June-2018 <br> Time: $\mathbf{3}$ hours <br> Digital Electronics \& Logic Design 

Max. Marks: 70
Note: Answer ALL questions in Part-A and any FIVE from Part-B
Part-A ( $10 \times 2=20 \mathrm{Marks}$ )

1. Implement the function $F=\left(x_{1}+x_{2}\right) \cdot x_{3}$ using logic gates.
2. Define SOP \& POS. Write the equivalent SOP expression for $\mathrm{F}(x, y, z)=x^{\prime} y+x z+y^{\prime} z$.
3. Define Multiplexer. Construct $4 \times 1$ multiplexer using $2 \times 1$ multiplexer.
4. Construct combinational circuit for a 2 bit multiplier.
5. Construct the circuit diagram of Gated $D$ latch. Write the truth table and excitation table.
6. Define Counters and draw Johnson counter logic diagram.
7. List out the differences between asynchronous and synchronous sequential circuit.
8. Define propagation delay, setup time and Hold Time of Flip Flop.
9. Illustrate the primitive flow table with example.
10. Discuss the significance of hazard?

Part-B $(5 \times 10=50 \mathrm{Marks})$
(All bits carry equal marks)
11. a) Implement the function $f=\left(x_{1}+x_{2}\right)\left(x_{2}+\overline{x_{3}}\right)$ using NOR gates.
b) Demonstrate by means of truth table the validity of the following identity $x+y z=(x+y)(x+z)$
12. a) Implement the following functions using PLA.
$f_{1}(a, b, c)=\sum(0,1,2,4) \quad f_{2}(a, b, c)=\sum(0,5,6,7)$
b) Design logic circuit of 2-to-4 decoder and write the VHDL code for the same.
13. a) Design 3-bit up counter. Explain its operation with timing diagrams.
b) Discuss about decoding problems in asynchronous sequential circuit.
14. a) List out the differences between Mealy and Moore models.
b) Design a synchronous counter with the repeated binary sequence $0 \rightarrow 2 \rightarrow 4 \rightarrow 6 \rightarrow 8 \rightarrow 0$ using $D$ flip flop.
15. a) Explain in detail steps for digital hardware modelling using CAD tools
b) Write notes on following terms:
i) Transition table ii) Flow table
16. a) Simplify the following Boolean function using Karnaugh map. $f(a, b, c, d, e)=\sum(0,2,4,6,9,13,21,23,25,29,31)$
b) Design Carry look ahead adder.
17. Answer any two of the following:
a) Compare Flip flops Vs Latches
b) Draw the logic diagram of ring counter. Explain its operation with timing diagram.
c) Draw the ASM chart for multiplying two 4 bit numbers. Explain its multiplication operation with numerical example.

